

# Unique IC's

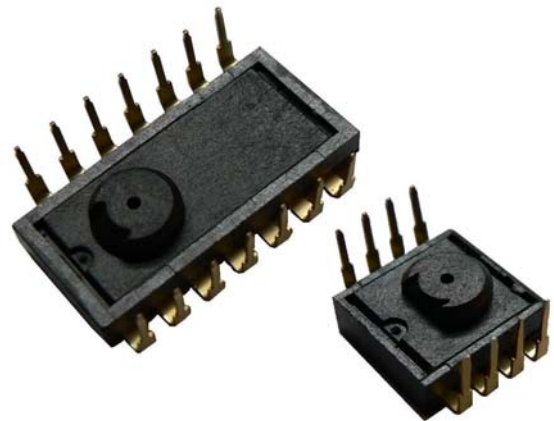
## UIC1003

### Solid-State Optical Mouse Sensor.

#### Data Sheet.

##### The main features.

- A fast response time. Maximum permissible speed of motion up to 6 m/s.
- Maximum permissible acceleration of motion up to 40000 m/s<sup>2</sup>.
- Maximum frame frequency up to 20000 frame/s.
- Super high resolution. It is capable to change resolution “on the fly” from 0 up to 5110 counts per inch (cpi) (any value multiple to 10).
- Low power consumption (less then 8 mW). 5 levels of power reduction at low speed of motion and at rest.
- Is ideal for use in optical mouse for wireless and game applications.



##### Functional Description.

The integral circuit (IC) UIC1003 is a reflective optical sensor that provides a non-mechanical tracking engine for implementing a standard mouse. It is based on optical navigation technology that measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement. UIC1003 has 2 variants of implementation:

1. UIC1003A – in 14-pin optical DIP package.
2. UIC1003B – in 8-pin optical DIP package.

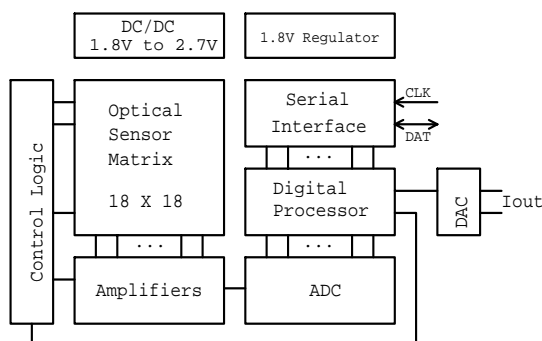


Fig. 1. Internal structure of IC UIC1003.

UIC1003 is used with an optical system and light emitting diode (LED) of infrared (IR) range. IC UIC1003 also need an external controller for communications with the computer both service of buttons and scroll.

Internal structure if IC UIC1003 is shown on fig.1. The basic block of IC is an optical matrix, containing 18×18 photosensitive cells. The image of surface, on which one goes the sensor, is focalized on a surface of an optical matrix, which one forms sequence of frames with frequency 20 kHz. The output signal from matrix is read out by the sample/hold amplifiers and digitized with the help of a 10-bit analog-to-digital converter (ADC).

Digital Processor calculates shift of the sensor by means of adjustment of two series frames. The adjustment is made by finding of a minimum of the norm of a difference of two frames using calculus of variations. The algorithm used permits calculate shift with accuracy, limited only by noise level of analogue block. With cell size of 50×50 um (which corresponds to resolution 500 cpi) shift calculations in digital processor is performed with accuracy 0.4 um (64000 cpi). The computed shift is normalized in accordance with the given resolution and than is transmitted to external controller through serial interface.

For normal algorithm operation it is necessary, that the value of shift behind one frame (50us) differed from predicted value of shift no more than on the size of an optical cell (50 microns). If the forecast is not conducted (i.e. the predicted shift is peer 0), the maximum speed of motion is equal to 1 m/s. At this condition the limit on the maximum value of acceleration is absent. If on the base of the speed, measured in previous frame, the forecast of shift is

conducted, there is a limitation on the value of the acceleration, which is equal to  $40000\text{m/sec}^2$ . Limitation on the maximum speed increases up to 6 m/sec, which is determined by design features of an optical matrix and algorithm. IC UIC1003 can operate in both modes. The choice of the mode of operation is performed through serial port from external controller.

From the said above it appears, that a major factor influencing on the maximum permissible speed of the sensor, is the frame frequency. Due to the large area of a cell and to special design of the readout circuit the optical matrix has high photosensitivity. It has allowed to raise frame frequency up to 20 kHz at relatively low level of a surface illumination (the LED current changes from 5 up to 20 mA, depending on the surface color). LED brightness adjustment, needed to support optimal signal level from optical matrix, is performed with the aid of build in digit-to-analog converter (DAC) with current type output. The DAC provides 16 levels of an output current in range from 200  $\mu\text{A}$  up to 30 mA. The level of a current varies in geometrical progression with a step  $\times 1.4$ .

Powering of UIC1003 is performed from the single voltage source VDD with output voltage range from 2 V to 3.5 V. Analogue parts of the IC and the digital core are powered from the build in voltage regulator with nominal output voltage 1.8V. Input/output circuits are powered immediately from input voltage source VDD. If during operation the value of VDD becomes lower, then minimum permissible level, internal circuit generates special internal signal PG=0. If IC UIC1003 is used in a wireless device, the signal PG can be read out through a serial port and utilized for indication of battery or accumulator discharge. Low level of minimum permissible voltage of power source ( $<2\text{V}$ ) allows completely to use energy of batteries and accumulators and to increase time of a continuous operation from one battery set.

In order to decrease power consumption all internal blocks of IC UIC1003 are operate in mode "Made and Sleep". All analogue blocks (sample/hold Amplifiers, ADC, timing diagram generator for optical matrix control) are powered only during operation of readout of recurrent frame from optical

matrix output. During exposition and in time intervals between frames, at decreased frame frequency they work in "sleep" mode. Current consumption decreases down to less than 1  $\mu\text{A}$ .

All blocks, included in digital processor, are supplied by clock signals only during implementation of particular operations. As CMOS devices in absence of clock signals do not contribute power, these measures allow significantly decrease power consumption, especially at low frame frequency, whenever the sensor speed is low.

At low speed of motion (when the sensor speed is less than 0.1 m/sec) the frame frequency may be lowered in 8 times. This leads to proportional decrease of power consumption. Switching in low frequency mode is performed automatically with the aid of build in block of frame frequency control.

If the sensor during long time is remaining at rest, subsequent step down lowering of frame frequency occurs (305 Hz, 38 Hz, 4.8 Hz, 0 Hz). This question will be considered verbosely in the section of operation modes description.

To ensure low level of fixed pattern noise from optical matrix, 2.7 V voltage source is required. It is used to form RESET signal for optical cells. The current contribution from this voltage source does not exceed 10  $\mu\text{A}$ . But if for this purpose to use voltage regulator, the requirement on the minimum level of input voltage VDD increases up to  $2.8\div 3\text{ V}$ . This greatly decreases extend of battery power use. To solve this problem build in DC/DC converter on the base of switched capacitors circuit is used. The input voltage of the converter is supplied from internal voltage regulator and equals to 1.8 V. Output voltage equals to 2.7 V. For ripple filtering external ceramic capacitor of  $0.1\div 1\ \mu\text{F}$  is required.

For communication with the external controller of the optical mouse the bi-directional serial interface is used. The information about calculated shift of the sensor along X, Y-axes is read out through this interface. Besides serial interface allows to read and to change configuration of the sensor, to change some parameters and the mode of operation. In more detail it is considered in section of the description of a serial port.

## Crystal structure and Package.

In fig.2 is shown layout view of the UIC1003. The figure shows size of the chip, PAD names and PAD numeration. The location of optical matrix center along vertical direction is exactly in the middle, and along horizontal direction it is shown in figure. The chip is placed in the package so, that the optical matrix center located exactly under optical window center.

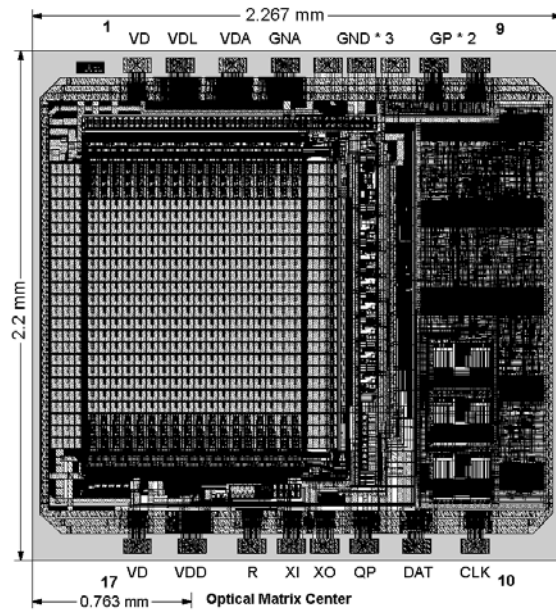
IC has 2 variants of implementation:

- 14-pin optical plastic DIP package – UIC1003A.

- 8-pin optical plastic DIP package – UIC1003B.

Chip has totally 17 external PAD's. Some PAD's are duplicated because its output currents may exceed 30 mA. Due to this circumstance 14 pins is enough for chip package.

In 8-pin variant of IC only internal generator and RESET circuit are used (see section of generator description). Hence one can't control the clock frequency by external resonator.



**Fig. 2. Common view of the chip of UIC1003.**

In table 1 are shown names and destination of the chip PAD's and its correspondence to PIN numbers for both variants of IC UIC1003.

**Table 1. Output destination of the IC UIC1003.**

PAD #	Name	Destination	PIN #	
			A	B
1	VD	The output of DC/DC converter +2.7 V.	1	-
2	VDL	Power Supply VDL = +1.8V for digital core.	2	1
3	VDA	Voltage regulator output. VDA= +1.8 V.	3	
4	GNA	Ground plane of analogue part of the IC UIC1003.	4	2
5	GND	Ground plane of digital part of the IC UIC1003.	5	3
6			6	
7				
8	GP	DAC output for LED powering.	7	4
9				
10	CLK	Clock input for built in serial port.	8	5
11	DAT	Data input/output for built in serial port.	9	6
12	QP	Control output of the LED current adjustment system.	10	-
13	XO	External clock generator.	11	-
14	XI	Normally they must be connected to ceramic or quartz resonator.	12	-
15	R	External power-up reset input.	13	-
16	VDD	Power Supply 2÷3.5 V.	14	7
17	VD	Parallel to PAD # 1.	-	8

**Table 2. Main electrical characteristics of the UIC1003.**

Parameter	Symbol	Min.	Norm.	Max.	Unit	Notes	
Power Supply Voltage	VDD	2.0	-	3.5	B		
Power Supply Current in modes:	I <sub>VDD</sub>				mA	At clock frequency 20 MHz	
1. Full Speed			3.6				
2. Low Speed			0.55				
3. Power Down 1			0.086				
4. Power Down 2			0.039				
5. Power Down 3			0.032				
6. Sleep			0.0017				
7. SAFE			0.55				
8. OFF		<0.001					
Optical Cell size	L		50		um		
Optical Matrix format			18×18				
LED operating wavelength	λ	600	860	900	nm		
ADC bit number	N <sub>ADC</sub>		10				
Resolution of the Sensor	Res	0	1000	5110	cpi	Any value multiple to 10. Default 1000	
Internal Clock generator frequency	F <sub>o</sub>	16	20	24	MHz		
External Clock generator frequency	F <sub>o</sub>	1	20	24	MHz	Determined by external resonator	
Frame frequency in "Full Speed" mode	F <sub>KADR</sub>		F <sub>o</sub> /1024				
Single Cell readout time	T <sub>CELL</sub>		2		T <sub>0</sub>	T <sub>0</sub> – clock period	
One Line readout time	T <sub>LINE</sub>		44		T <sub>0</sub>		
Full frame readout time	T <sub>KADR</sub>		839		T <sub>0</sub>		
Maximum permissible speed of motion:	V <sub>MAX</sub>				m/sec	At clock frequency 20 MHz in "Full Speed" mode	
1. With predictions			6				
2. Without predictions		1					
Maximum permissible acceleration:	A <sub>MAX</sub>				g		
1. With predictions			4000				
2. Without predictions		∞					
Input signal level:	Input Low (logical "0") Input High (logical "1")	V <sub>IL</sub> V <sub>IH</sub>	0 VDD - 0.5		0.5 VDD	V	Inputs CLK, DAT, R, XI
Output signal level:	Input Low (logical "0") Input High (logical "1")	V <sub>OL</sub> V <sub>OH</sub>	0 VDD - 0.5		0.5 VDD	V	Outputs DAT, QP, XO

Parameter	Symbol	Min.	Norm.	Max.	Unit	Notes
DAC output current range (for LED brightness adjustment)	$I_{LED}$	0.2		32	mA	16 current levels. $I_{n+1} = I_n \times 1.4$
Serial Port clock frequency	$F_{CLK}$	0.01		10	MHz	
Build in voltage regulator output voltage	VDA		1.8		V	@ VDD>2 V
DC/DC converter output voltage	VD		2.7		V	External filtering capacitor 1÷10 uF
ESD	$V_{BR}$	350			V	All pins, Machine Model
Operating temperature	$T_{OP}$	0		50	°C	
Storage temperature	$T_{ST}$	-40		85	°C	

### Main operation modes of the UIC1003.

In the table 3 the list of the main operational modes of UIC1003 is added. Depending on operation mode changes frame frequency, on-off time ratio of LED, operation mode of voltage regulator and clock generator. In power down modes, when current consumption decreases down to 100 uA and lower, voltage regulator is switched in power saving mode. In this mode its own current consumption reduces from 10 uA down to 1.7 uA.

For an estimation of total consumption of an IC UIC1003 together with the external light emitting diode the data on LED current consumption are given. It is assumed, that the sensor is moving on the surface similar to a white paper. The full current consumption of the optical mouse, including USB mouse controller, will depend on a type of the controller used together with sensor.

**Table 3. Operation Modes of UIC1003.**

Mode name	Frame frequency	Internal block operation mode			Current consumption			Mode ON condition	Mode ON delay	Mode OFF condition
		LED on-off time ratio	Voltage Regulator 1.8 V.	Generator	UIC1003	LED	Total			
<b>Full Speed</b>	20 kHz	1	Full Power	On	3.6mA	7mA	10.6mA	–	0	–
<b>Low Speed</b>	2.44 kHz	0.125÷1	Full Power	On	550uA	0.88mA	1.43mA	$V < V_o$	1.68 sec.	$V > V_o1$
<b>Power Down 1</b>	305 Hz	1/64	Power Down	On	86uA	110uA	196uA	MOV=0	53.7 sec.	MOV=1
<b>Power Down 2</b>	38.15 Hz	1/512	Power Down	On	39uA	14uA	53uA	MOV=0	7m.10 sec.	MOV=1
<b>Power Down 3</b>	4.77 Hz	1/4096	Power Down	On	32uA	1.7uA	34uA	MOV=0	28m.38 sec.	MOV=1
<b>SLEEP</b>	0	Off	Power Down	Off	1.7uA	0	1.7uA	SCLK=1	53.7 sec.	SCLK=0
<b>OFF</b>	0	Off	Off	Off	0	0	0	from SP	0	from SP
<b>SAFE</b>	2.44 kHz	0.125	Normal	On	550uA	1.25mA	1.8mA	$N > 2^{N_{bad}}$	0	$N > 2^{N_{safe}}$

Main operation mode of UIC1003 is a “**Full Speed**”. If calculation of the shift is performed with predictions on the base of the current value of speed, maximum permissible speed is equal to  $V_{MAX} = 6m/s$ , and maximum permissible acceleration –  $a_{MAX} = 40000m/s^2$ . If predictions by speed are suppressed, than maximum permissible speed diminishes down to  $V_{MAX1} = 1m/s$ , and maximum permissible acceleration –  $a_{MAX1}$  is not limited. After initial RESET the mode of calculation without predictions is established. For actuation of predictions by speed it is necessary through a serial port to record logical “1” in 4-th bit of configuration register **RG\_config** (its address is equal to 112, the wait of the bit is equal to 8<sup>1</sup>). The read and write procedure for serial port is explicitly considered in section of a serial port description.

At realization of certain conditions the control circuit automatically switches an IC in a power saving mode. The first level of a power consumption decrease is the “**Low Speed**” mode. In this mode the

frame frequency and accordingly power consumption (including LED) diminishes in 8 times. The mode of predictions by current value of speed at shift calculations in “**Low Speed**” mode is always switched off. Maximum permissible value of speed in “**Low Speed**” mode is equal to  $V_{MAX1} = 12.5cm/s$ , and maximum acceleration –  $a_{MAX1}$  is not limited. Automatic switch in a “**Low Speed**” mode occurs at speed  $V < V_o$ , where  $V_o = (6m/s)/2^{N_{ref}}$  and  $N_{ref}$  – is the number, saved in the initial state register (its address is equal to 121). After initial ESET it is established to value 15. Its value may be changed by means of serial port. Return to “**Full Speed**” mode occurs at condition  $V > V_o$ . At the initial moment after IC powering a “**Low Speed**” mode is established, as the speed of the sensor is not yet calculated and the state of all registers is zeroed.

If IC is in a “**Low Speed**” mode and along 53.7s the shift in both directions stay equal to 0, the “**Power Down 1**” mode is switched. The frame frequency and the power consumption are decreased else in 8 times (in comparison with “**Low Speed**” mode). If in the process of shift calculation any value of shift in any direction is detected, immedi-

<sup>1</sup> Hereinafter addresses and data are given in a decimal code. The lower bit of data is considered as 1-st.

ately switch in “Full Speed” mode occurs. In similar way but with more long delays occurs switch in modes “**Power Down 2**”, “**Power Down 3**”. Exit from these modes is the same as for previous one.

For shift detection in modes “**Power Down 1, 2, 3**” in worse case one may need the time which is equal to frame period. At the moment of switch in “**Full Speed**” mode the sensor speed cannot exceed 1m/s (since the sensor speed is not yet calculated and it is considered be equal to 0, i.e. the mode of a prediction by speed has not included yet). Thus, the acceleration at escaping a power down mode should not exceed:

$$A_{PDN} = (1m/s) \cdot F_{KADR}.$$

If IC is stay in “**Power Down 3**” mode and an external controller stops read/write operations through serial port (i.e. CLK input stay in high level state), then with 53.7s delay the “**SLEEP**” mode is switched on. In “**SLEEP**” mode all analogue blocks are switched of add generator is stopped. The only block, contributing current is a voltage regulator. Total current consumption not exceeds ~1.7 uA. UIC1003 cannot exit from “**SLEEP**” mode in a result of shift, as the calculation of shift in this mode is not performed. Exit from “**SLEEP**” mode occurs at any access to serial port, for example, after re-sumption of reading data about shift. If an optical mouse, using IUC1003, proved in “**SLEEP**” mode, the user can break this state by pressing any button.

The last step in power lowering is a mode “**OFF**” – shutdown of all internal blocks. The mode “**OFF**” is switched on/off by writing from external controller through the serial port logical “1”/”0” in bit 5 of register RG\_CON (address 111).

In “**OFF**” mode the voltage 1.8 V is not more suspended by build in voltage regulator. So, if a digital core (powering pin VDL) is powered from build in voltage regulator 1.8 V (output pin VDA), it is required to take some measures to prevent dropping of VDL lower then 1.2 V when you use “**OFF**” mode.

For some applications switching in power saving modes may be undesirable, as it decreases operation speed. If UIC1003 is used in USB-mouse for game applications, power consumption has no meaning, but operation speed lowering may be critical. For such cases UIC1003 does support external control by operation modes by means of internal register RG\_CON. Address of register RG\_CON is equal to 111. Bit 5 of the register, as mentioned above, controls the IC switching in “**OFF**” mode. Bit 4 controls “**Full Speed**” mode. When bit 4 is set high, switching of UIC1003 in power saving modes is disabled. IC operates only in “**Full Speed**” mode. Bit 3 if set high forces switching in “**Low Speed**” mode. Bit 4 and bit 5 must be low in this case. If bit

3 is set high, internal control by frame frequency is turned off. To return IC in a “**Full Speed**” mode one must reset bit 3 of the register RG\_CON.

Bit 2 of register RG\_CON when set high prohibits transition in modes “**Power Down 1, 2, 3**”. In this case there are two possible operation modes – “**Full Speed**” and “**Low Speed**”.

IC UIC1003 has an opportunity to set mode “**SLEEP**” from external controller. This command is executed by writing any number in the register with address 127. Switching in “**SLEEP**” mode occurs immediately after writing without time delay. To return IC in “**Full Speed**” mode one must to write or to read any register with any address except 127.

The last of possible operation modes is a “**SAFE**” mode. This mode is used when the optical mouse is raised from the desktop. When the user raises the optical mouse, a rotary motion of mouse body occurs. This leads to a quick shift of picture and may course an abrupt jump of cursor in arbitrary direction. To eliminate this effect, at the moment of raising from the desktop an IC is switched in a “**SAFE**” mode. In the “**SAFE**” mode calculated value of the shift is zeroed. This prevents any movement of cursor, when the mouse is raised from the desktop. The frame frequency in the “**SAFE**” mode is 8 times lower, then in “**Full Speed**” mode.

To detect the moment of raising from the desktop the digital processor continuously checks the quality of picture. The quality of picture is checked up by three criterions. The current frame is believed as bad if one of the three conditions is executed:

1. Picture contrast is lower, then a minimum permissible value –  $D_{MIN}$ .
2. The signal level in most bright point of picture is lower, then a minimum permissible value –  $Q_{BAD}$ .
3. Difference between predicted and calculated value of shift is greater then a maximum permissible value –  $XY_{MAX}$ .

Besides, external controller can set attribute **Bad\_Frame** = 1 (register RG\_CON, address 111, bit 1). In this case the current frame is also believed as bad. If  $2^{N_{bad}}$  successive frames are bad, IC is switched in a “**SAFE**” mode. In a “**SAFE**” mode digital processor continues calculation of the shift, but this information does not transferred to the output. Return to “**Full Speed**” mode occurs, when  $2^{N_{safe}}$  successive frames have normal quality.

Numbers  $N_{BAD}$ ,  $N_{SAFE}$ ,  $D_{MIN}$ ,  $Q_{BAD}$ ,  $XY_{MAX}$  are keeping in initial set registers and may be changed through the serial port. To check current mode of operation is possible by reading of register “**Motion**”. More detailed information about addresses and format of these registers is given in section of serial port description.

### System of the Picture brightness control.

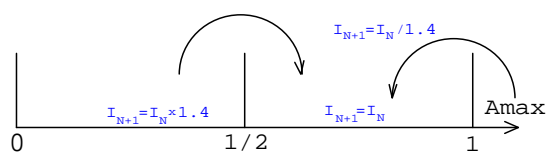
When the sensor moves along desktop surface, the level of signal from optical matrix output

strongly depends on optical characteristics of the surface. The level of signal from white and black

paper differs in 15÷20 times. If LED brightness is constant, the level of signal on black surface is insufficient for normal operation of calculation algorithm. To ensure the normal operation of an IC on arbitrary surfaces the system of auto-adjustment of LED brightness will be used. The powering of LED is performed from digital-to-analogue converter (DAC) with current type output. Depending of input code DAC provides 16 levels of output current in the range from 0.2 to 30 mA. The scale of output current is exponential. Each successive value of current is in 1.4 times greater, then the previous one. Besides, at low frequencies signal level adjustment may be performed by exposition length.

UIC1003 can operate with different types of LED with red and infrared radiation. A positive outlet of LED is connected to power source VDD, and a negative one – to the output of the DAC (pin with name GP). Minimum power contribution gives the use of high efficient infrared LED. With LED of type L-7113SF6C ( $\lambda=860$  nm) together with optical system of firm “Agilent” (or with its analogue) on the white paper saturation of output signal from optical matrix occurs at current 10mA, and mean operating current amounts 7 mA (at frame frequency 20 kHz).

In “**Full Speed**” mode exposition length is always equal to frame period. In “**Power Down 1, 2, 3**” modes exposition length stay the same as in “**Full Speed**” mode. The on-off time ratio of LED current is equal to the coefficient of frequency lowering. In “**Low Speed**” mode on-off time ratio of LED current may be changed from 1/8 to 1 and takes one of the following meanings: 1/8, 3/16, 1/4, 3/8, 1/2, 3/4, 1. Manly in “**Low Speed**” mode is used on-off time ratio 1/8. Brightness regulation is performed by the value of current. If the current achieves its maximum value but the output signal is not enough, the increase of on-off time ratio occurs.



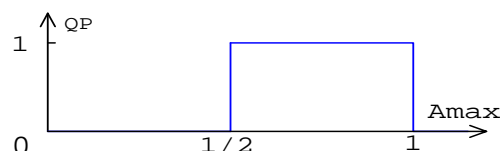
**Fig. 3. Operation algorithm of Brightness adjustment system.**

As an input information for a brightness adjustment system the signal from the most bright point of the frame serves. If output signal in most bright point is less, then 0.5 of ADC full scale, the LED current is increased in 1.4 times. If even at one point of the frame the output signal is in saturation, LED current decreases in 1.4 times. This algorithm is shown in fig.3.

### Shift calculation module.

Shift calculation algorithm allows calculate the shift of the sensor with very high resolution. In prac-

Brightness adjustment system forms auxiliary output signal QP (see fig. 4). This signal serves as an indicator of normal picture brightness. If the level of output signal is in optimal range (from 0.5 to 1 of ADC scale), the signal QP=1. This signal is useful for test purposes. Additionally it may be used for powering auxiliary external LED, which will indicate normal operation conditions. When the desktop surface is too dark for normal operation, auxiliary LED will be switched off. Signal QP can be read in **Motion** register (address 2, bit 7). In an IC version UIC1003A this signal is taken out on an external pin QP.



**Fig. 4. Output check signal QP.**

If necessary, the LED current established at some time moment, it is possible to control from the outside controller. Input code of the DAC is 4 bits long. It can be read in the register **DAC\_TEST** to the address 110 (lower 4 bits of the register **DAC\_TEST** represent input code of the DAC). Code 0 corresponds to minimal output current of the DAC (200 uA), code 15 corresponds to maximal output current of the DAC (30 mA).

Besides, in UIC1003 is supported the possibility to control DAC output current from external controller. For this purpose the register **DAC\_CON** is used. Its address is equal to 110. If bit 5 of the register **DAC\_CON** is set high, the DAC is controlled by external code from controller. This code must be written in bits 1÷4 of the same register. When bit 5 is reset low, the DAC is controlled by the code from the brightness adjustment system. Bit 6 of the register **DAC\_CON** controls the LED on/off switching (0 – switch on, 1 – switch off). Bit 6 is active only when the bit 5 is set high.

If UIC1003 operates under external brightness control, the information about optical matrix output signal level is need. Signal QP gives not enough information. In this case one can use information from the statistical processing block. In this block one can read information about maximum signal level in last frame (address 100), minimum signal level in last frame (address 99) and mean signal level in last frame (address 101). More detailed information about the statistical processing block is given in section of serial port description. Considered capabilities may be useful for testing of final production on the stage of manufacturing and exploitation.

tice the noise level limits maximum achievable resolution. Total noise level depends not only from the

quality of analogue part of IC. Significant contribution to total noise can give some external factors such as LED noise, the quality of PCB-board, used for amounting UIC1003 and other components of the electrical circuit, the quality and location of filtering capacitors. Increased level of noise can result in cursor jittering, which is most visible at low speed of motion. In order to achieve high resolution in combination with high performance dynamic noise filtering is used.

Shift calculation algorithm includes 3 steps. The first step – is a current speed calculation (the speed on the time interval between last and previous frame). Second step – is a current speed filtering. For this purpose second order I2R-filtr is used. Due to the filter the noise level is reduced on 30 db. Third step – is speed integration. As the response time of the filter is much more, than the frame period, information on sharp and fast movements of the sensor will be transmitted to the output with large delay. Therefore, speed integrator has two parallel channels. The fast channel integrates non-filtered value of speed. The slow channel integrates filtered value of speed. When the speed of the sensor is low, the difference between outputs of these two channels is negligible. As the speed of the sensor increases, absolute value of the difference rises. If the sensor stopped, some time later the difference becomes equal to 0.

The principle of a dynamic filtration consist in switching of the output register between fast and slow channels depending on the absolute value of the difference between them. When the absolute value of difference is lower, then some given value  $Th_{ON}$ , the output register is switched to the slow channel output. This means, that the filter is switched on. If the absolute value of difference is lower, then some value  $Th_{OFF}$ , the output register is switched to the fast channel output, i.e. the filter is switched off.

When the sensor remain at rest or moves with slow speed, the cursor jitter is good visible. In this situation the filter is switched on and the cursor jitter is eliminated. At the same time the filter does not influence on the accuracy of the shift calculation. At high speed of motion the jitter is practically non-visible. So, the filter is switched off, as it significantly distorts output signal. The use of dynamic filtration allows to achieve high accuracy of shift calculation in full speed range and to attenuate the noise influence.

For the filter setup the registers  $T_F$ ,  $T_{FF}$ ,  $Th_{ON}$ ,  $Th_{OFF}$  are used. Registers  $T_F$ ,  $T_{FF}$  (addresses 119, 120) are used for tuning of the time constant of the 1-st and the 2-nd stages of the filter. Time constant is equal:  $T = T_{FRAME} \cdot 2^{Tf}$ , where  $T_{FRAME}$  – frame period. Registers  $Th_{ON}$ ,  $Th_{OFF}$  (addresses 125, 126) determine the thresholds of on/off switching of the filter.

As a length unit at shift calculation the size of the optical cell is used (50 um). So, the base resolu-

tion is equal to 500 cpi. But the accuracy of calculation amounts 1/128 of length unit. This permits to change output resolution in wide range from 0 to 64K. If the result of shift calculation is simply rounded, output resolution equals to 500 cpi. If calculated shift is divided by 500 then multiplied by M and rounded, output resolution will be equal to M. In IC UIC1003 one can to set any value of resolution from 0 to 5110 multiple to 10. Output resolution M is controlled by the number  $N_{RES} = M/10$ .  $N_{RES}$  – is a 9-bit number from 0 to 511. The lower 8 bits of number  $N_{RES}$  are stored in register **Resolution** (address 118). The upper bit of number  $N_{RES}$  is stored in register **RG\_config** (address 112, bit 5). After initial power up reset on default  $N_{RES} = 100$ . Accordingly, output resolution  $M = 1000$  cpi. The value  $N_{RES}$  at any moment can be changed from external controller through the serial port.

Calculated shift along X, Y-axes is stored in registers **Delta\_X**, **Delta\_Y**. The number of bits of these registers is equal to 8. Data notation is signed 2's complement. Maximum permissible range is from -128 (binary code: 100...0) up to +127 (binary code: 011...1). If calculated shift exceeds these limits, the overload signal is set high. The information about overload is stored in the register **Motion** (address 2). Besides, in this register is stored information about presence or absence of shift in any direction since last reading of registers **Delta\_X**, **Delta\_Y** and information about operation mode. Format of the register **Motion** is following:

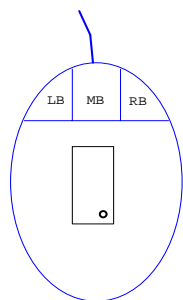
Bit #	Bit name	Notes
<b>Bit 1:</b>	LSP=1	– IC operate in a “ <b>Low Speed</b> ” mode.
<b>Bit 2:</b>	PDN=1	– IC operate in one of the modes “ <b>Power Down 1, 2, 3</b> ”.
<b>Bit 3:</b>	PG=0	– the voltage level of power source VDD is less then minimum permissible value.
<b>Bit 4:</b>	OVR <sub>Y</sub> =1	– overload along Y-axis.
<b>Bit 5:</b>	OVR <sub>X</sub> =1	– overload along X-axis.
<b>Bit 6:</b>	SAFE=1	– IC operate in a “ <b>SAFE</b> ” mode (see hereinbefore).
<b>Bit 7:</b>	QP=1	– the level of signal from optical matrix is normal.
<b>Bit 8:</b>	MOV=0	– the shift in both directions since its last reading is equal to 0.

Reading of the data from registers **Delta\_X**, **Delta\_Y** may be synchronous and asynchronous. At asynchronous data reading information about shifts along X and Y-axis is read independently. As the external controller is not synchronized with frame frequency, reading of the shift along X-axis may occur in one frame period, and along Y-axis – in another one. During this time in **Delta\_Y** register may be added new information about the shift in last frame. This means, that X-coordinate was read for one point and Y-coordinate – for another point. At high speed of motion and at high resolution this can significantly distort data about trajectory of the sen-

sor. To avoid this effect, 2 synchronous read modes are added. X-synchronized reading assumes reading at first of shift along X-axis, and then shift along Y-axis. When **Delta\_X** register is read, the shift along Y-axis is stored in **Delta\_Y** register and does not change until **Delta\_Y** register is read. Similarly at Y-synchronized reading at first **Delta\_Y** register is read and then **Delta\_X** register.

The choice of necessary mode of reading is performed by address. At asynchronous reading addresses of **Delta\_X**, **Delta\_Y** registers are equal 3 and 4 accordingly. At X-synchronized reading addresses of **Delta\_X**, **Delta\_Y** registers are equal 8 and 9 accordingly. In this mode **Delta\_X** register is read first, **Delta\_Y** register – second. At Y-synchronized reading addresses of **Delta\_X**, **Delta\_Y** registers are equal 11 and 10 accordingly. In this mode **Delta\_Y** register is read first, **Delta\_X** register – second.

For correct transfer of the data about shift in computer well-defined orientation of the chip on PCB is required.



**Fig. 5. Recommended location of IC UIC1003 on PCB.**

Fig. 5 shows recommended orientation of IC package on PCB. On the figure conditionally is shown the body of optical mouse, the place of buttons location and the place of an output of wire, connecting the mouse with computer. IC package is shown by black rectangle. A round mark shows the location of the first pin of IC. At given orientation the direction of the cursor motion on the monitor screen corresponds to the direction of mouse motion on the desktop.

Sometimes may appear a necessity to rotate IC package. IC UIC1003 allows rotation by any angle multiple to 90°. If the IC package is rotated by 180°, the shift in both directions changes sign. At rotation by ±90° it is necessary to swap X and Y-axes and to change sign along one of the axes. These operations

can be easily performed with the aid of register **RG\_config** (address 112). Format of the **RG\_config** register is shown below:

Bit #	Bit name	Notes
<b>Bit 1:</b>	Swap=1	– swap of X, Y axes.
<b>Bit 2:</b>	invX=1	– inversion of the shift along X-axis.
<b>Bit 3:</b>	invY=1	– inversion of the shift along Y-axis.
<b>Bit 4:</b>	PR <sub>ON</sub> =1	– switch on the mode of the shift calculation using predictions by current speed (sets maximum permissible speed 6 m/s).
<b>Bit 5:</b>	HI <sub>RES</sub> =1	– the mode of high resolution (upper bit of number N <sub>RES</sub> ).

**RG\_config** register is available for read and write operations. After initial power up reset the value of **RG\_config** register by default is established equal to 0.

Combination of high resolution and high operating speed requires a special approach to communication with computer. Ordinary the data transfer through USB-port occurs by 8-bit words with frequency from 20 to 200 times/s. At resolution 1000 cpi maximum speed, at which overload not occurs, equals to 64 sm/s. For this reason optical mice with maximum permissible speed 1m/s or greater require special driver. Some users utilize special program, which enables to increase the frequency of data transfer up to 1000 times/s.

Standard protocol of data transfer for USB-mouse provides possibility to transmit information about shift along X and Y-axes by 16-bit words. In order to realize all ability of UIC1003 concerning operation speed and resolution, mouse USB-controller must suspend extended transfer protocol. Besides, one must take into account that if the sensor is moving with maximum permissible speed 6 m/s at maximum resolution 5110 cpi, registers **Delta\_X**, **Delta\_Y** are overloaded during 106 us, which corresponds to 2 frames. This requires to set the frequency of data transfer to external controller not lower than 9500 times/s. If it is planned to use UIC1003 with maximum resolution M [cpi] and maximum speed V[m/s], frequency of data transfer with mouse controller F[times/s] must be determined in accordance with expression:

$$F = 0.3076 \times V \times M$$

### **Clock generator and initial RESET.**

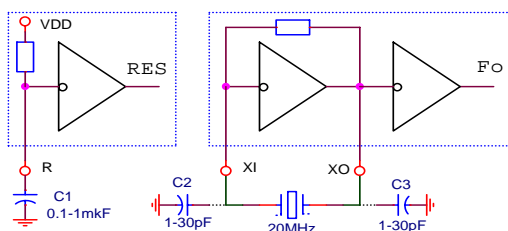
IC UIC1003 has 2 sets of clock generator and power up reset block – internal and external. At any time can operate only one of these 2 sets. The choice of required set is performed by connection of pin R.

The set of external clock generator and power up reset uses external elements, which determine clock frequency and RESET-signal duration. Its internal

structure and schematic diagram of connecting external elements is shown in fig.6. RESET-signal duration is determined by time constant of RC-circuit, consisting of external capacitor C1 and internal resistor (R = 400 kΩ).

Clock frequency is determined by nominal frequency of external quartz or ceramic resonator, con-

nected to pins XI, XO. If ceramic resonator is used, two additional external capacitors C2, C3 must be connected to ensure normal operation of generator. IC UIC1003 can operate with resonators from 1 MHz to 20 MHz.



**Fig. 6. Schematic diagram concerning external generator and reset circuit.**

At clock frequency lowering proportionally decreases power consumption and maximum permissible speed and acceleration. As UIC1003 has a good speed resource, for some applications (for example, for wireless mouse) may be reasonably to reduce frequency. This increases the time of continuous operation from one battery set at the expense of speed lowering.

The set of internal clock generator and power up reset uses build in RC-circuits, which determine clock frequency and RESET-signal duration. Internal generator has fixed frequency 20 MHz  $\pm$ 20%. The RESET-signal duration equals to  $\sim$ 16ms. The use of internal clock generator and power up reset deprives user the possibility to change clock frequency. But this diminishes the number of external elements, excludes 3 external pins and permits to use package with 8 pins. The use of internal clock generator significantly diminishes power consumption, especially in modes “**Power Down 2, 3**”, because in these modes the main part of power contribution gives clock generator. Internal clock generator contributes only about 30  $\mu$ A because its output does not connected to external pins. Due to high PAD capacitance external generator contributes not lower than 200  $\mu$ A. If ceramic resonator is used instead of quartz the situation is bad worse. Ceramic resonator requires additional capacitors C2, C3, connected to pins XI, XO. Its nominal may reach 30 pF. It is easy appreciate, that at voltage swing 0.5 V at pin XI and 1.5 V at pin XO at frequency 20 MHz current contribution of this capacitors amounts to 1.2 mA. For this reason at clock frequency 20 MHz to ensure low power consumption in modes “**Power Down 2, 3**”, which is shown in table 3, is possible only with internal clock generator.

The choice of internal or external clock generator is performed by pin R connection. When pin R is

connected in accordance with schematic diagram, shown in fig.6, than the set of external clock generator and power up reset is used. If instead of capacitor C1, pin R is connected to VDD, than the set of internal clock generator and power up reset is used. In this case capacitors C1÷C3 and resonator are not required. When internal generator is used, pin XI is automatically tied to pin GND with the aid of build in key. The pin XO in this case must be free.

The main condition of the choice of internal generator is that at the moment of IC powering pin R is tied to VDD. If IC UIC1003 operates with internal generator and pin R on some time is tied to low level, the switch on external generator occurs. Back switch cannot be performed while power is switched on.

It is worth to mention the possibility to use an external clock signal (for example, from external controller). In this case pin R is connected according to fig.6, and external clock signal is connected to pin XI. Elements C2, C3 and ceramic resonator are excluded.

IC UIC1003 is manufactured in 2 implementation variants. Variant UIC1003A is packaged in 14-pin plastic DIP-package, where chip pads R, XI, XO are connected to corresponding pins. This variant permits to use internal generator, as well as external one. The other implementation variant – UIC1003B is packaged in 8-pin DIP-package. In this variant pad R is internally connected to input VDD. This variant permits to use only internal generator and power up reset.

To test the frequency of the clock generator is possible through register GEN<sub>TEST</sub> (address 109). It allows to calculate the number of clock pulses, coming for a given time interval. To start test procedure one must to write number 1 in register GEN<sub>TEST</sub>. At this moment the counter is cleared and starts clock pulses counting. Some time later command “Stop” is given by writing number 0 in register GEN<sub>TEST</sub>. At this moment the counter is stopped and its contents may be read at the same address 109. If time interval between the end of “Start” command and the end of “Stop” command equals 5  $\mu$ s, to frequency 20 MHz will correspond number 100.

Another method to test clock frequency Fo is to measure frame frequency. If IC is switched in “**Low Speed**” mode, the signal on LED will be switched with frame frequency  $F_{FR} = F_o/8192$ . The procedure of switching UIC1003 in “**Low Speed**” mode is in detail considered in the section of operation modes description (see above).

### Build in voltage regulators.

Powering of IC UIC1003 is performed from a single voltage source  $V_{DD} = 2\div 3.5$  V. All the other

voltages required for IC operation are generated with the aid of build in DC/DC converters.

IC UIC1003 has 4 internal power buses:

1.  $VDD = 2\div 3.5V$  – is used for powering input/output circuits and built in voltage regulator. This bus is connected immediately to external power source  $VDD$ .
2.  $VDA = 1.8V$  – is used for powering of analogue part of IC. This bus is connected immediately to the output of built in voltage regulator. For noise and crosstalk reduction it must be connected to external filtering capacitor through the pin  $VDA$ . The value of capacitor is in range  $5\div 20\mu F$ .
3.  $VDL = 1.8V$  – is used for powering of digital core. Pin  $VDL$  may be powered from independent external voltage source  $+1.8V$ , but typical application implies its connection to pin  $VDA$ . Owing to external filtering capacitor crosstalk from digital part does not influence of the analogue part. In implementation variant UIC1003B chip pads  $VDA$  and  $VDL$  are connected to common external pin  $VDA$ , which must be connected to filtering capacitor.
4.  $VD = 2.7V$  – is used for powering of reset pulse generator for optical matrix. This bus is connected immediately to the output of built in DC/DC converter. Pin  $VD$  must be connected to external ceramic capacitor with nominal capacitance  $1\div 10\mu F$ .

Built in voltage regulator converts voltage from  $VDD$ -source to stabilized voltage  $+1.8V$ . It consists of reference voltage source differential amplifier and powerful output transistor. Regulator provides output current up to  $15mA$ . Input voltage regulation is less than  $0.001$ , output current regulation  $<1V/A$ . Minimum voltage drop across the regulator is less than  $200mV$ . So, the minimum input voltage is equal to  $2V$ .

Its own current contribution equals to  $10\mu A$ . When IC UIC1003 operates in modes “**Power Down 1, 2, 3**” voltage regulator is switched in low power mode in which its own current contribution decreases down to  $1.7\mu A$ . Besides, regulator has an “**OFF**” mode in which its contribution equals to  $0$ .

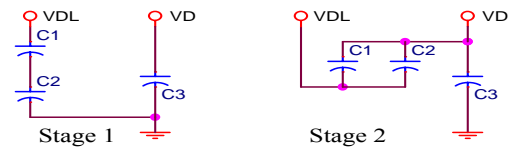
### Serial input/output port.

For data exchange with the external controller in a structure of an IC UICD1003 the bidirectional serial port is included. The port executes 3 main functions:

1. Data transfer about shifts along X, Y-axes to external controller.
2. Programming of IC parameters, checking and control by operational modes from the external controller.
3. IC testing.

For communication with the external controller the 2-wire line –  $CLK, DAT$  – is used. Timing signal  $CLK$  for IC UICD1003 is input and is always controlled from the external controller. Signal  $CLK$

DC/DC converter transforms  $+1.8V$  in to  $+2.7V$ . It is made on the base of switched capacitors. Its operation principle is shown in fig.7. Converter uses clock signal. In one of the phase of clock signal internal capacitors  $C1, C2$  connected in series are charged till voltage  $V_{DL}=1.8V$ . Each of capacitors is charged till  $V_{DL}/2=0.9V$ . In the other phase they are switched in parallel between  $VDD$  and  $VD$ . External capacitor  $C3$  serves to smooth voltage pulsation. Output voltage is equal to  $VD = V_{DL} \times 1.5$ . As a clock signal for DC/DC converter optical matrix line read signal is used. External capacitor  $C3$  should be placed as close to pin  $VD$ , as possible. Moreover, it should have low internal impedance at high frequencies. It is recommended to use only ceramic or tantalum capacitors.



**Fig. 7. Operation principle of DC/DC converter (multiplier by 1.5).**

To minimize noise and crosstalk level all filtering capacitors, connected to power pins, should be located as close to proper pins as possible. Connecting lines on PCB should be wide and short. It is necessary to remember, that electrolytic capacitors have large internal impedance at high frequencies due to inductive component of impedance. If electrolytic capacitors are used, one must to put ceramic capacitor with nominal value  $0.1\div 1\mu F$  in parallel.

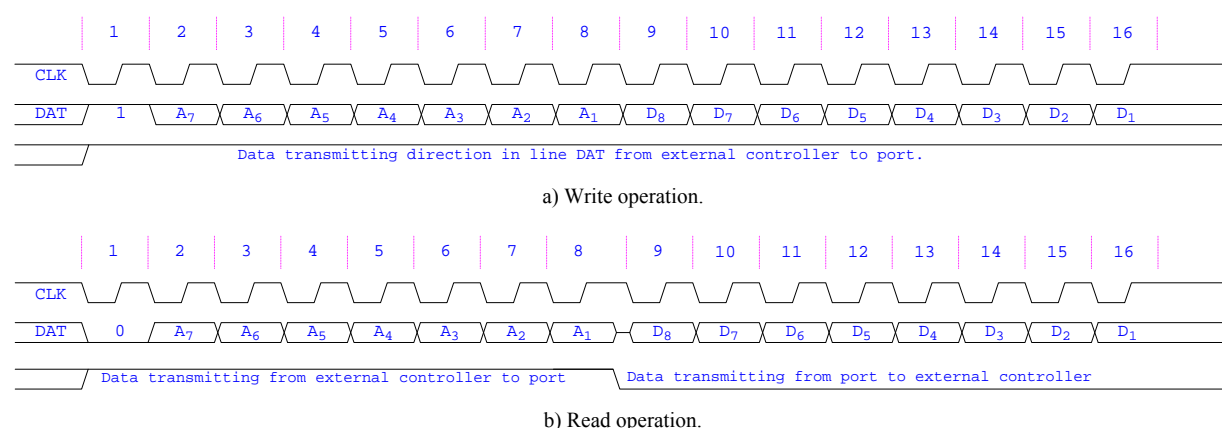
The special attention should be given to a common bus (GND). To ensure maximum resolution of optical mouse it is desirable to have a two-layer PCB, on which one of the layers will be used predominantly for distributing the common bus GND, at least, around of a IC UIC1003 and filtering capacitors.

can be as synchronic in relation to an internal clock of an IC, and asynchronous. The line  $DAT$  is bidirectional. The format of the transmitted data is an 8-bits word. The standard data read/write cycle takes 16 clock ticks of a signal  $CLK$  and starts with transfer of an opcode. Then 7 bits of the address are transmitted. The initial 8 clock ticks the data transition through line  $DAT$  always occurs from the external controller to an IC UIC1003. If in the pause between data transfer the line  $DAT$  was under IC UIC1003 control, on the first negative front of  $CLK$  line  $DAT$  is released and passes under control of the external controller.

Next 8 clock ticks data transfer occurs. The transmitting direction through line  $DAT$  depends on

a type of operation. When the data transfer finishes, signal CLK is set to high level. Line DAT keep its

last state and transfer direction till next data transfer cycle.



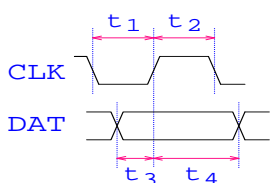
**Fig. 8. Timing diagram for write (a) and read (b) operations.**

Fig.8a shows timing diagram for write operation. Initially port is set in the wait state. In first cycle of signal CLK through line DAT the opcode 1 is transmitted. Than 7 bits of address are transmitted. The upper bit is transmitted the first, the lower bit – the last. Next 8 cycles the data are transmitted, beginning with upper bits.

delay between negative edge of CLK and data change on line DAT (see fig.10 and table 4). After data read is finished line DAT keep its state and remain under serial port control till the next negative edge on line CLK.

**Table 4. Timing diagram requirements.**

Name	Symbol	Min.	Norm	Max.	Unit
CLK pulse duration.	$t_1$	25			ns
Intervals between CLK pulses.	$t_2$	25		100000	ns
Data set time before active CLK front.	$t_3$	10			ns
Data hold time after active CLK front.	$t_4$	10			ns
Data delay time.	$t_5$			15	ns

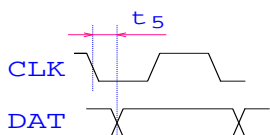


**Fig. 9. Write operation timing requirements.**

Data receiving occurs on positive edge of signal CLK. Fig.9 together with table 4 show timing requirements on minimum data set and data hold time.

Most difficult conditions for port operation appears during read operation in cycle 8 at time interval  $t_2$  (see fig.8b, fig.9). By positive edge on line CLK the last bit of address is received. Then the address received is decoded and the signal of addressed register reading is formed. Till the negative edge of CLK information from the register asked should come on internal 8-bit data bus. As the number of registers connector to internal data bus is large, considerable time delay occurs. Just this delay set conditions for minimum value of time interval  $t_2$ . It is possible to increase the speed of data transfer through the serial port if during read operation in cycle 8 time interval  $t_2$  is increased in comparison with other cycles.

Address and data received are temporary stored in the buffer registers. By positive edge of last pulse CLK the record in one of internal registers with according address occurs. At the same time port is set in wait state till next operation.



**Fig. 10. Read operation timing requirements.**

Fig.8b shows timing diagram for read operation. Operation code transmitted in first cycle is equal to 0. Then external controller transmits address of the register to be read and releases line DAT. The address received is decoded and data from appropriate register are written in a shift register by negative edge of 9-th CLK pulse. At the same time ICs serial port captures line DAT. The data change on line DAT during read operation by the negative edge on line CLK occurs. Data read is characterized by time

One of the problem of 2-wire interface is the problem of synchronization. In 3-wire interface adding of signal “Frame”, which shows the start and stop of each read/write operation, solves this problem. In 2-wire interfaces synchronization during the power up reset occurs. Further synchronization is suspended with the aid of counter. After each 16 pulses on line CLK port is set in the wait state. Such exchange protocol assumes full absence of crosstalk on line CLK and errors in counter operation, which is not always happen in practice. To ensure coherent operation of serial port IC UIC1003

uses additional internal block for synchronization. Operation of this block is founded on the fact, that the pause between exchange cycles is as a rule much longer than time intervals between pulses inside a read or write operations. Block has a counter operating from internal clock generator. It measures the duration of time intervals when the line CLK is in a high level state. If pause between CLK pulses exceeds  $T_{SPRES}$ , serial port is set in a wait state even if the previous exchange operation was not finished. At the same time the line DAT is released and is set to be ready to receive data. The length of interval  $T_{SPRES}$  amounts from 4 to 5 frames or from  $4096 \cdot T_o$  to  $5120 \cdot T_o$ , where  $T_o$  – is a period of internal gen-

erator clock signal ( $T_{SPRES} = 204.8 \div 256$  us at  $F_o = 20$  MHz).

This ensures synchronization with external controller if data exchange frequency not exceeds 4K times/s. If data exchange frequency is high it is recommended periodically to test serial port. For testing may be used a special register **TEST** (address 7). It is available for write and read operations. If the read information does not coincide with written data the pause with duration not less than  $T_{SPRES}$  should be inserted after serial port testing. The testing of serial port may also be performed by reading of **Product\_ID** or **Revision\_ID** registers. These registers are available only for read operation. Its addresses and data saved are given in next section in table 5.

### Internal registers of UIC1003.

The list of all internal registers of IC UIC1003 is given in table 5. Initial value, shown in the table means the register contents which is established after power up reset. Operation type means available for the given register directions of data transfer: RD – possibility of data read from register, WR – possibility to write data in to register. Independently of

the register length all read/write operations transfer 8 bits of data in accordance with exchange protocol. If the register length is less than 8 bits at read operation upper bits may take arbitrary value. One should to mask unused bits to prevent error. At write operation unused bits can be set to an arbitrary level.

**Table 5.** List of internal registers of UIC1003.

Name	Address	Bit number	Initial value	Operation type	Destination
<i>The working general-purpose registers.</i>					
<b>Product_ID</b>	0	8	56	RD	Identification code of a product. The readable value is equal 56.
<b>Revision_ID</b>	1	8	3	RD	Version number. The readable value is equal 3.
<b>Motion</b>	2	8	x	RD	The information on availability of shift, overload and operational modes. Format of the register: {MOV, QP, SAFE, OVR <sub>x</sub> , OVR <sub>y</sub> , PG, PDN, LSP}
bit 1			1		<b>LSP</b> = 1 – IC operates in mode “ <b>Low Speed</b> ”.
bit 2			0		<b>PDN</b> = 1 – IC operates in one of the mode “ <b>Power Down 1, 2, 3</b> ”
bit 3			x		<b>PG</b> = 0 – supplied voltage VDD is not enough for normal operation.
bit 4			0		<b>OVR<sub>y</sub></b> = 1 – shift along Y-axis exceeds permissible limits.
bit 5			0		<b>OVR<sub>x</sub></b> = 1 – shift along X-axis exceeds permissible limits.
bit 6			0		<b>SAFE</b> = 1 – IC operates in mode “ <b>SAFE</b> ”.
bit 7			x		<b>QP</b> = 1 – image brightness is normal.
bit 8			0		<b>MOV</b> = 0 – The shift along both axes from time of last reading is equal to 0.
<b>Delta_X</b>	3, 8, 11	8	0	RD	Shift along the X-axis, which has occurred from time of the previous reading. After reading the register is automatically reset.
<b>Delta_Y</b>	4, 9, 10	8	0	RD	Shift along the Y-axis, which has occurred from time of the previous reading. After reading the register is automatically reset.
<i>The registers for initial pre-sets.</i>					
<b>RG_config</b>	112	5	0	RD/WR	Configuration register. Format: { HI <sub>RES</sub> , PR <sub>ON</sub> , invY, invX, Swap }
bit 1			0		<b>Swap</b> = 1 – swap axes X-Y
bit 2			0		<b>invX</b> = 1 – inversion along X-axis
bit 3			0		<b>invY</b> = 1 – inversion along Y-axis
bit 4			0		<b>PR<sub>ON</sub></b> = 1 – enable predictions by speed
bit 5			0		<b>HI<sub>RES</sub></b> = 1 – increase resolution by 2560
<b>Resolution</b>	118	8	100	WR	Mouse resolution – M. $M = (HI_{RES} \cdot 256 + Resolution) \times 10$ cpi
<b>D<sub>MIN</sub></b>	113(low) 114(hi)	16	50	WR	Minimum acceptable contrast of image for a quality monitoring system. Is written by 2 bytes: lower byte - low, upper byte - hi.
<b>XY<sub>MAX</sub></b>	115	8	192	WR	Maximum permissible value of a fractional part of shift ( $\times 128$ ).
<b>Tau</b>	117	4	3	WR	Time constants of averaging of speed for the block of predictions.
<b>T<sub>F</sub></b>	119	4	6	WR	Time constants of 1-st stage of the filter.
<b>T<sub>FF</sub></b>	120	4	10	WR	Time constants of 2-d stage of the filter.

Name	Address	Bit number	Initial value	Operation type	Destination
<b>N<sub>REF</sub></b>	121	4	15	WR	If in a normal mode the number of frames, passed without change of reference frame, exceeds $2^{N_{ref}}$ , forced change of reference frame occurs.
<b>NI<sub>REF</sub></b>	122	4	4	WR	The same as Nref, but for SAFE mode.
<b>N<sub>BAD</sub></b>	123	4	5	WR	If $2^{N_{bad}}$ successive frames are bad, IC is switched in SAFE mode.
<b>N<sub>SAFE</sub></b>	124	4	6	WR	If in SAFE mode $2^{N_{safe}}$ successive frames are bad, IC is switched in NORMAL mode.
<b>Th<sub>ON</sub></b>	125	8	6	WR	Threshold of actuation of output filter.
<b>Th<sub>OFF</sub></b>	126	8	16	WR	Threshold of deactivation of output filter.
<b>The registers for mode control.</b>					
<b>RG_CON</b>	111	5	0	WR	Register format: {OF, FulSP, LowSP, FulPWR, Bad_Frame } <b>Bad_Frame</b> =1 – indicator of bad frame for a picture quality monitoring system. <b>FulPWR</b> =1 – prohibition of switching in “Power Down 1, 2, 3” modes. <b>LowSP</b> =1 – switches IC in “Low Speed” mode (without delay) <b>FulSP</b> =1 – switches IC in “Full Speed” mode. Dominate over bit LowSP. <b>OF</b> =1 – full switching-off of IC (switching in mode “OFF”). Dominate over bits FulSP, LowSP
bit 1			0		
bit 2			0		
bit 3			0		
bit 4			0		
bit 5			0		
<b>SET_SLEEP</b>	127	–	–	WR	The record of any number in the given register transfers the scheme in a “SLEEP” mode.
<b>Registers for internal blocks testing.</b>					
<b>TEST</b>	7	8	x	WR/RD	Write and read of any number for Serial Port testing.
<b>GEN<sub>TEST</sub></b>	109	8	x	WR/RD	Generator frequency measurement. The register stores number of clock pulses counted in a given time interval. Command <b>START</b> (Write 1): resets and starts pulse counter. Command <b>STOP</b> ( Write 0): stops counter and stores its data in GEN <sub>TEST</sub>
<b>DAC<sub>TEST</sub></b>	110	4	x	RD	Reading of a code coming on a DAC from a brightness regulation system.
<b>DAC<sub>CON</sub></b>	110	6	x	WR	External DAC control. Format : { led_of, dac_test , t_DAC[4-1] }
bit 1÷4		4	x		<b>t_DAC</b> – Code coming on a DAC at condition: <b>dac_test</b> = 1
bit 5			0		<b>dac_test</b> = 0 – DAC control from a brightness regulation system.
bit 6			0		<b>dac_test</b> = 1 – DAC control from register DAC <sub>CON</sub>
					<b>led_of</b> = 1 – LED off (is active only at <b>dac_test</b> = 1)
<b>2-level comparator of the data read through the serial port.</b>					
<b>CMP<sub>MIN</sub></b>	0	8	x	WR	The lower limit of a comparator range.
<b>CMP<sub>MAX</sub></b>	1	8	x	WR	The upper limit of a comparator range
<b>CMP<sub>OUT</sub></b>	6	8	x	RD	The result of comparison. Format: {(6×True), nHI, nLOW } <b>nLOW</b> = 0 – if DATA < <b>CMP<sub>MIN</sub></b> , <b>nLOW</b> =1 – if DATA ≥ <b>CMP<sub>MIN</sub></b> <b>nHI</b> = 0 –if DATA > <b>CMP<sub>MAX</sub></b> , <b>nHI</b> =1 – if DATA ≤ <b>CMP<sub>MAX</sub></b> <b>True</b> =1 – if <b>CMP<sub>MIN</sub></b> ≤ DATA ≤ <b>CMP<sub>MAX</sub></b>
bit 1					
bit 2					
bit 3÷8					
<b>Moving picture generator.</b>					
<b>PIC<sub>GEN</sub></b>	104	7	2	WR	Control register for moving picture generator. Format: {absV, VS <sub>Y</sub> , V <sub>Y</sub> , VS <sub>X</sub> , V <sub>X</sub> , MATR <sub>ON</sub> , GEN <sub>ON</sub> }
bit 1			0		<b>GEN<sub>ON</sub></b> =1 – switch on moving picture generator.
bit 2			1		<b>MATR<sub>ON</sub></b> =1 – enable optical matrix signal adding to total picture.
bit 3			0		<b>V<sub>X</sub></b> = 0/1 – speed along X-axis equals to 0/(1 cell/frame) (1 m/s)
bit 4			0		<b>VS<sub>X</sub></b> =0/1 – speed along X-axis positive/negative
bit 5			0		<b>V<sub>Y</sub></b> = 0/1 – speed along Y-axis equals to 0/(1 cell/frame) (1 m/s)
bit 6			0		<b>VS<sub>Y</sub></b> =0/1 – speed along Y-axis positive/negative
bit 7			0		<b>absV</b> =1 – switch on absolute value of speed integration mode.
<b>PIC<sub>AMP</sub></b>	105	8	255	WR	Register for the test picture amplitude control. Brightness of dark dots is equal to 0. Brightness of white dots is equal to <b>PIC<sub>AMP</sub></b>
<b>PIC<sub>FAZ</sub></b>	106	4	0	WR	Register for picture shift control. Format: { SHS <sub>Y</sub> , SH <sub>Y</sub> , SHS <sub>X</sub> , SH <sub>X</sub> }
bit 1					<b>SH<sub>X</sub></b> = 0/1 – shift picture along X-axis by 0/1 dot (50 um)
bit 2					<b>SHS<sub>X</sub></b> =0/1 – picture shift along X-axis is positive/negative
bit 3					<b>SH<sub>Y</sub></b> = 0/1 – shift picture along Y-axis by 0/1 dot (50 um)
bit 4					<b>SHS<sub>Y</sub></b> =0/1 – picture shift along Y-axis is positive/negative
<b>The registers of the statistical processing block.</b>					
<b>ADC<sub>CON</sub></b>	96	3	6	WR/RD	Control register of statistical block. Format: { BAD <sub>CON</sub> , Sum, STAT <sub>ON</sub> }
bit 1			0		<b>STAT<sub>ON</sub></b> =1 – block of statistical processing is switched on.
bit 2			1		<b>Sum</b> = 0 – mode of measurement of a mean noise on a current cell.
bit 3			1		<b>Sum</b> = 1 – mode of measurement of a mean noise on a full frame. <b>BAD<sub>CON</sub></b> =1 – switch on the picture quality monitoring using value of <b>ADC<sub>MIN</sub></b>

Name	Address	Bit number	Initial value	Operation type	Destination
<b>ADR<sub>LOW</sub></b>	97	8	x	WR	Lower byte of the current cell address.
<b>ADR<sub>HI</sub></b>	98	8	x	WR	Upper byte of the current cell address.
<b>ADC<sub>LOW</sub></b>	97	8	x	RD	Lower byte of current cell data – DATA[8-1].
<b>ADC<sub>HI</sub></b> bit 1÷2 bit 3÷7 bit 8	98	8	x x 0 1	RD	Upper 2 bits of current cell data and ready-bit. Format: { notREDY , 0 , 0 , 0 , 0 , 0 , DATA[10-9] } <b>DATA[10-9]</b> – upper 2 bits of current cell data. Zeros <b>notREDY</b> =0 – current cell data are ready.
<b>ADC<sub>MIN</sub></b>	99	8	0	RD	Minimum data value in current frame. Format: {DATA <sub>MIN</sub> [10-3]}
<b>ADC<sub>MAX</sub></b>	100	8	255	RD	Maximum data value in current frame. Format: {DATA <sub>MAX</sub> [10-3]}
<b>ADC<sub>SUM</sub></b>	101	8	0	RD	Current value of total sum on frame. Format: {SUMMA[19-12]}
<b>ADC<sub>STD</sub></b>	102	8	0	RD	Mean absolute value of noise
<b>Q<sub>BAD</sub></b>	100	8	70	WR	Minimum permissible value of <b>ADC<sub>MAX</sub></b> for picture quality monitoring.

The main registers used at operation with optical mouse listed in section of general-purpose registers. Registers **Product\_ID** and **Revision\_ID** are used only for initial identification of a product after IC powering. The reading of the information about shifts is made in the registers **Motion**, **Delta\_X**, **Delta\_Y**. Immediately after reading the information about shifts according registers are reset to 0. Accordingly are reset bits MOV, OVR<sub>X</sub>, OVR<sub>Y</sub> of the register **Motion**. For this reason register **Motion** should be read the first. Otherwise the information about overload will be loosed. If along some of the axes X or Y overload occurs in according register (**Delta\_X**, **Delta\_Y**) is placed the number +127 or –128, depending on the direction of the shift.

Next register group – initial pre-set registers – allows to change IC parameters and to perform tuning of shift calculation process parameters for optimal combination of sensitivity and response speed. By default IC is tuned on the resolution 1000 cpi and maximum permissible speed 1m/s (maximum acceleration is not limited). Configuration register is

set so that direction and sign of axes X, Y corresponds to package location on PSB in accordance with fig.5.

To increase maximum permissible speed up to 6 m/s it is necessary to set high bit PR<sub>ON</sub> in the register **RG\_config**. The choice of required resolution is performed through the register **Resolution** and bit HI<sub>RES</sub> of the register **RG\_config** in accordance with equation given in table 5. If the output resolution is set near its maximum value, correction of the low-pass filter parameters (T<sub>F</sub>, T<sub>FF</sub>) may be required.

The registers of mode control enable to interfere in the operation of internal IC mode control system from outside controller. They allow to disable switching in a “**Low Speed**”, “**Power Down**”, “**SLEEP**” and “**OFF**” modes or conversely to force switching in these modes.

The other registers are assigned mainly for test purposes. As IC testing has significant meaning not only in the IC manufacture process but also at the stage of final production control its capabilities are separately considered in a next section.

## Registers for internal block testing.

### Serial port testing.

Prior to internal block testing it is necessary to check serial port itself. For this purpose internal register **TEST** is intended. It allows writing and reading of any 8-bits numbers. For normal operation of serial port it is not required internal clock 20 MHz, i.e. testing of serial port may be performed before clock generator testing. The only requirement to other blocks of IC during serial port testing is a low level of signal RESET. If internal set of clock generator and block reset is used the duration of RESET-signal amounts about 16 ms. Accordingly after an IC powering on a delay not less then 20 ms should be made before start of serial port testing. If external set of clock generator and block reset is used the duration of RESET-signal is defined by external capacitor or immediately by external RESET-signal source. The minimum duration of a signal RESET should provide the setting of voltage VDL up to a nominal level taking into account filtering capacitors.

### Clock generator testing.

Next module, which can be tested after serial port, is a clock generator. For this purpose is used register **GEN<sub>TEST</sub>**. In this register is kept the number of clock pulses passed during a given time period. Command START (writing number 1 to address 109) resets the counter and starts counting. Command STOP (writing number 0 to address 109) stops the counter and writes its contents in **GEN<sub>TEST</sub>** register. Check time interval during which the counter operates lasts from the end of command START till the end of command STOP. Then the contents of the register **GEN<sub>TEST</sub>** can be compared with upper and lower limits.

### Build in 2-level digital comparator.

Modern testing concept is based on the comparison of timing diagrams measured on IC outputs with a reference one. Such test procedure can only compare the read data with a specific number and answer the question “equal or not equal”. But it cannot answer the question whether the read data DAT sat-

isfy equation  $DATA_{MIN} \leq DAT \leq DATA_{MAX}$  or not. To solve this problem the digital comparator is introduced in the structure of serial port. It contains the registers  $CMP_{MIN}$ ,  $CMP_{MAX}$  and  $CMP_{OUT}$ . Upper and lower limits are written in registers  $CMP_{MIN}$ ,  $CMP_{MAX}$ . Any time when some data are read through the port (accept the register  $CMP_{OUT}$ ) these data are compared with upper and lower limits and the result of comparison is saved in the register  $CMP_{OUT}$ .

#### Picture brightness control block testing.

Registers  $DAC_{TEST}$  and  $DAC_{CON}$  enable to test brightness adjustment block and analogue block in whole including optical matrix and ADC. With the aid of register  $DAC_{TEST}$  the code coming on DAC from brightness adjustment system is checked. Register  $DAC_{CON}$  enables to control the DAC output current from external controller. The switching from internal to external control is performed by setting high of bit  $dac\_test$  of the register  $DAC_{CON}$ . When  $dac\_test = 1$  output current of the DAC is determined by 4 lower bits of the register  $DAC_{CON}$ . In this mode is possible LED switch on/off by means of set/reset bit  $led\_of$  of the register  $DAC_{CON}$ . The reacting of an optical matrix to LED brightness variation can be tested with the help of the statistical processing block, which enables to read image from optical matrix, to read minimum, maximum and mean brightness of the image.

#### Module of statistical processing.

This block enables to read full image from the output of optical matrix and get some statistical information, which characterize main parameters of the image. Besides the block participates in picture quality control, which one was already mentioned above. The list of the module functions is resulted below:

1. Full image read.
2. Measurement of the maximum level of the current frame brightness.
3. Measurement of the minimum level of the current frame brightness.
4. Measurement of the mean level of the current frame brightness.
5. Measurement of the noise level at any point of frame.
6. Measurement of the full noise level of frame.
7. Picture quality monitoring.

Immediately after IC powering on only one of the listed functions is switched on. It is a picture quality monitoring. As a criterion of picture quality the level of maximum picture brightness –  $A_{MAX}$  is used. The value  $A_{MAX}$  is compared with the number  $4 \times Q_{BAD}$ , where  $Q_{BAD}$  – is a content of the register  $Q_{BAD}$ . If  $A_{MAX} < 4 \times Q_{BAD}$ , the frame is believed as bad. Picture quality monitoring may be switched off via resetting to “0” of bit  $BAD_{CONT}$  of the register  $ADC_{CON}$ .

Switching on of others functions is performed by setting to “1” bit  $STAT_{ON}$  of the register  $ADC_{CON}$ .

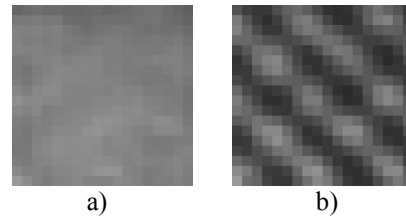
To read full image 2 pairs of registers  $ADR_{HI}$ ,  $ADR_{LOW}$  and  $ADC_{HI}$ ,  $ADC_{LOW}$  are used. The first one is used for address storing and the second – for data storing. All cells in an optical matrix are numerated in the order of their read from 0 till 323 (18 lines with 18 cells in each line). In accordance with this numeration each cell has its own address. The cell located in line number L (from top) and in row number R (from left) will have address:

$$ADR = (R-1) + 18 \cdot (L-1)$$

The cell which has address, stored in an address register ( $ADR_{HI}$ ,  $ADR_{LOW}$  register pair) is considered as current cell. Each time when an ADC converts output signal from the current cell these data are stored in the data register ( $ADC_{HI}$ ,  $ADC_{LOW}$  register pair).

As an ADC output is a 10-bits word and data register is a 16-bits word, upper 6 bits of the register  $ADC_{HI}$  are equal to 0 when the data are stored. But when an address is changed stored data become non-actual and the upper bit of the register  $ADC_{HI}$  is set high. This property is used to check data availability. When a next address is set one should first to read register  $ADC_{HI}$ . If upper bit of the data read is equal to 1, this means that the data are not ready. But when the upper bit becomes equal to 0 the data are ready and one should read the register  $ADC_{LOW}$ .

Maximum time required to read data since the data are ready including writing next address amounts 80 CLK pulses. So the full image read may be performed with the frequency 540 frames/s.



**Fig. 11. Surface image obtained on a white (a) and on a contract (b) paper.**

Fig.11 shows 2 examples of the image read on different surfaces. Apart from analogue part testing full image read may be used to check an optical system focusing.

The value of minimum, maximum and mean image signal level through the last frame can be read in registers  $ADC_{MIN}$ ,  $ADC_{MAX}$  and  $ADC_{SUM}$  correspondently. Its contents are updated in each frame after finishing read of last frame. In order to agree the data capacity in the registers  $ADC_{MIN}$ ,  $ADC_{MAX}$  are written 8 upper bits of ADC output (lower 2 bits are rejected which is equivalent dividing by 4).

To calculate mean image signal level the sum through whole frame is calculated. Calculated value should be divided by 324 (the number of cells in frame) and then by 4 (to agree the data capacity). To simplify calculations the sum is divided by 2048 (i.e. 11 lower bits of the result are rejected). So, to

find mean image brightness one should multiply the content of the register  $ADC_{SUM}$  by coefficient:

$$K_{SUM} = 2048/324 = 6.321$$

Register  $ADC_{STD}$  is used to measure noise level. As a root mean square (RMS) noise calculation requires significant hardware cost in statistical processing block mean absolute value of noise is calculated. Depending on distribution function mean absolute noise amounts  $0.8 \div 0.87$  of RMS noise which is enough for approximate noise estimation. For averaging first order low-pass filter is used with time constant amounting 128 frames.

Depending on the state of bit **Sum** of the register  $ADC_{CON}$  current cell noise or total noise across full optical matrix is measured. The result of noise calculation appears with time delay about  $150 \div 200$  frames after the command on noise measurement was send.

At current cell noise measurement the difference between 2 successive frame signals from current cell is used as a noise signal. This means that a single cell noise is multiplied by 1.41. Besides at storing in the register  $ADC_{STD}$  calculated value is multiplied by 4. Taking into account mentioned above coefficient  $0.8 \div 0.87$  final coefficient for noise calculation is equal to  $K_{NOISE(CELL)} = 4.53 \div 4.92$  :

$$NOISE_{CELL} = ADC_{STD}/K_{NOISE(CELL)}$$

At total noise measurement the difference between 2 successive frame signals sum is used as a noise signal. If the noise of separate cells is not correlated total noise is  $18 \times 1.41$  times greater than the mean noise of a single cell. At storing in the register  $ADC_{STD}$  the result is divided by 8. Taking into account coefficient  $0.8 \div 0.87$  final coefficient for noise calculation is equal to  $K_{NOISE(SUM)} = 2.55 \div 2.77$  :

$$NOISE_{MEAN} = ADC_{STD}/K_{NOISE(SUM)}$$

#### **Moving picture generator.**

Full-scale both IC and optical mouse testing requires to project with the aid of optical system some picture on the surface of optical matrix and emulate its motion, which is a complex technical task. To solve the problem of testing without using additional equipment build in generator of moving picture is used.

This generator digitally synthesizes the chess-board like picture. The contrast of the picture can be adjusted from 0 to 255. The picture may be static or moving in one of the 8 directions with the speed 1 cell/frame (1 m/s). The static picture may be shifted by single cell (50  $\mu$ m) in any direction. Digitally generated picture may be linearly summed with the picture from optical matrix. If the surface of optical

matrix is uniformly illuminated by the LED without any optical system one can create picture background where era taken into account all matrix defects (fixed pattern noise, black and white points, electrical noise and the like). This background is summed with digitally generated picture of any required contrast. So we can emulate situations when the sensor is at rest or is shifted by 50  $\mu$ m in any direction or is moving with the speed 1m/s in any direction. And final picture includes real noise and other defects of analogue part.

Generator operation is controlled by 3 registers –  $PIC_{GEN}$ ,  $PIC_{AMP}$ ,  $PIC_{FAZ}$ . Their destination is described in table 5. In common mode operation bit  $MATR_{ON}$  of the register  $PIC_{GEN}$  should be set high to enable passing analogue picture to digital processor. Picture contrast is adjusted by register  $PIC_{AMP}$ . Register  $PIC_{FAZ}$  enables to shift picture by 50  $\mu$ m in any direction.

Register  $PIC_{GEN}$  has additional bit **absV** not associated directly with moving picture generator. This bit allows measuring output noise of the shift calculator. This noise does depend on the ratio of analogue block noise to picture contrast. If bit **absV**=1, output integrators begin integrate absolute value of speed along axes X and Y. Integration lasts during 20 frames. Then accumulated sum is stored in registers **Delta\_X**, **Delta\_Y** and new cycle of integration begins.

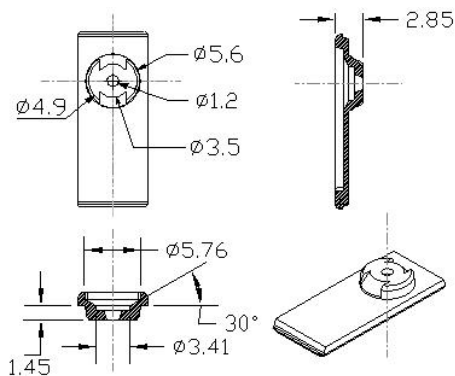
Output noise measurement function operates independently from picture generator. When the final production is tested it is possible to measure cursor jittering when the mouse is at rest on different surfaces. When IC is tested (without optical system) moving picture generator and background optical matrix illumination with LED should be switched on. Moving picture generator must operate in static pattern mode. After bit **absV** is set high one must make a pause about 20 frames and read the registers **Delta\_X**, **Delta\_Y**. The data delivered it is necessary divide by 20 and multiply by  $0.8 \div 0.87$ , i.e. totally one must divide data by 16. Space scale corresponds to resolution, specified by the register **Resolution**. If maximum available value of resolution is established (5110 cpi) during output noise measurement the lower bit of the data delivered corresponds to 0.32  $\mu$ m of RMS noise (corresponds to resolution 81760 cpi). If noise measured on some surface equals for example to 5, the RMS noise equals to 1.56. Maximum achievable resolution on this surface equals to  $81760/5=16352$  cpi.

### **Optical system choice.**

For IC UIC1003 optical system is required. Optical system performs 2 functions: focuses the image of the desktop on the surface of optical matrix and illuminates the surface of the desktop with the aid of the LED. For compatibility with UIC1003 optical system must satisfy 2 requirements. The join unit of

an optical system should on a design and sizes be compatible with an IC package optical cover. The image of the desktop on which the sensor is moving should exactly be focused on an optical matrix surface. Conjunctive parameters of optical window on

an IC package cover, which is joined with optical system, are shown in fig. 12.



**Fig. 12. Package cover outline drawing.**

Among most widely used optical systems which are compatible with UIC1003 is an optical system developed by the firm Agilent or similar to it. Its



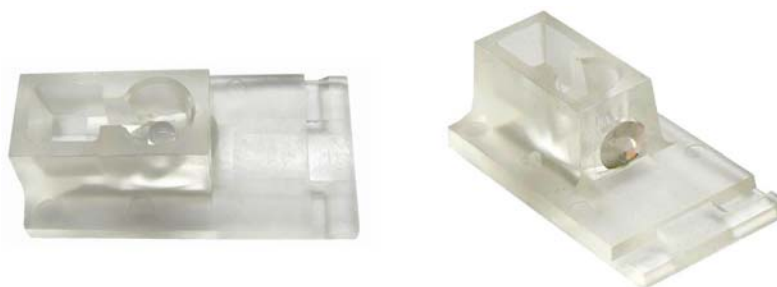
**Fig. 13. Optical system consistent with UIC1003 from Agilent.**

Another type of optical system, which can be used together with IC UIC1003, is an optical system developed by the firm Unique ICs. Its general view is shown in fig.14. This is a coaxial-type optical system. Its main feature is a vertical illumination of a desktop surface. General advantage of such approach is a much higher LED efficiency. At lateral

general view is shown in fig.13. This is a lateral-type optical system with two separate optical channels. It contains two lenses. The main lens which is used to project desktop image on the optical matrix surface has a vertical optical axis. For desktop surface illumination auxiliary lens on one side of optical system is used.

The main feature of this type optical system is a lateral illumination of a desktop surface. LED light falls on the desktop at large angle relative vertical axis. If there is a micro-relief of a surface it allows to boost an image contrast due to lateral shadows arising at lateral light dropping. High image contrast increases signal/noise ratio during shift calculation. Due to this obstacle Agilent optical system enables sensor to operate on wide range of surfaces excluding glossy and mirror-type surfaces.

illumination main part of an incident light flow is reflected outside optical channel. Only small part of LED radiation energy diffused from desktop hit upon optical matrix. In Unique ICs optical system LED radiation illuminates desktop surface vertically and main part of the light energy returns in optical system and hit upon photo-receiver.



**Fig. 14. Coaxial type optical system consistent with UIC1003 from Unique ICs.**

Owing to vertical illumination operating LED current using Unique ICs optical system is 2÷3 times lower than with Agilent optical system at equal other conditions. As it is seen from table 3 LED current contribution amounts most part of the total current contribution. So Unique ICs optical system enables about 2 times decrease total power consumption of optical mouse in comparison with Agilent optical system employment.

Main disadvantage of vertical illumination is an image contrast lowering which leads to increased signal to noise ratio. As a result on a homogeneous surfaces an increased level of output noise cause cursor jittering, which finally force the user to reduce mouse resolution.

Coaxial type optical systems with vertical illumination are most attractive for laser mice. Use of coherent radiation enables to achieve very high im-

age contrast due to light interference at vertical illumination. But a high level of noise of laser LED's not allows to achieve as high resolution as with a common LED light.

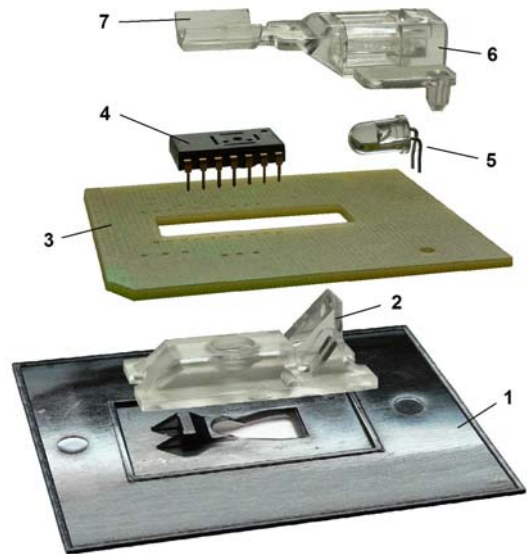
An ultimate optical system choice depends on an optical mouse implementation variant. For USB optical mouse an Agilent optical system is more preferable to use because it ensures normal operation on a wide range of surfaces. On the other hand a high level of LED current, which is need with Agilent op-

tical system, is not critical for USB-mouse. But for wireless optical mouse power consumption is a key factor for user. Unique ICs optical system enables 2 times increase the continuous operation time from one battery set. In order to keep high resolution of the mouse a special high contrast light-reflecting pad for optical mouse is need. For many users power saving variant of wireless optical mouse can appear more preferential.

### Common design requirements.

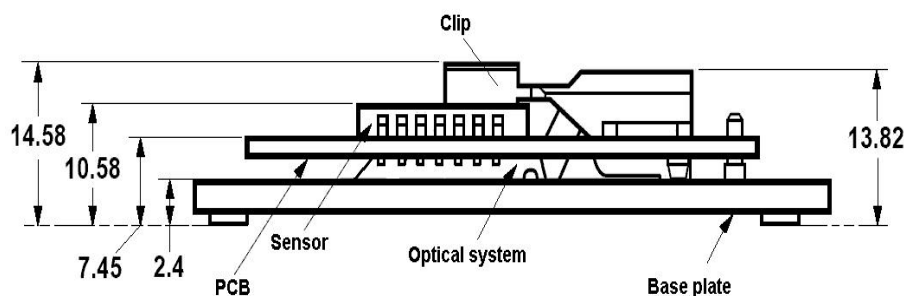
Fig. 15 shows arrangement of optical mouse using UIC1003. Main design elements are: base plate of mouse body (1) optical system (2), PCB (3), motion sensor IC UIC1003 (4), light emitted diode (5), clip (6). IC is mounted on a PCB so that IC outputs by its wide part touch the PCB surface. PCB has a cut through which an optical system is closely touched to IC package. The clip holds the LED in relation to the optical system lens to provide uniform illumination of the surface. The LED should be inserted into the clip and LED's leads formed before mounting on PCB. Clip has a plastic spring (7). Its under side is pressed to IC package and upper side – to mouse body cover. It provides compression of all design along a vertical axis, that is the relevant condition for exact desktop image focusing on an optical matrix surface.

For exact focusing the main lens of optical system should be located at certain distances from desktop and chip surfaces. The required distance from the lens to the chip surface ensures close pressing of the optical system to an IC package cover. The required distance from the lens to the desktop is adjusted by the base plate thickness and by an additional packing on an under side of the base plate (see fig.16).



**Fig. 15. Optical Mouse arrangement.**

The basic design sizes of the optical mouse general assembly using Agilent optical system is shown in fig.16.



**Fig. 16. Assembly drawing using Agilent optical system.**

If a Unique ICs optical system is used the LED should be mounted on an under PCB side. The clip has another construction and executes the same functions. Fig 17 shows the basic design sizes of the optical mouse general assembly using Unique ICs optical system.

Figures 18 and 19 show outline package dimensions for IC's UIC1003A and UIC1003B respectively.

Fig. 20 shows a PCB fragment draft recommended for IC UIC1003A, Agilent optical system, LED and clip mounting. Fig.21 shows the same for UIC1003B.

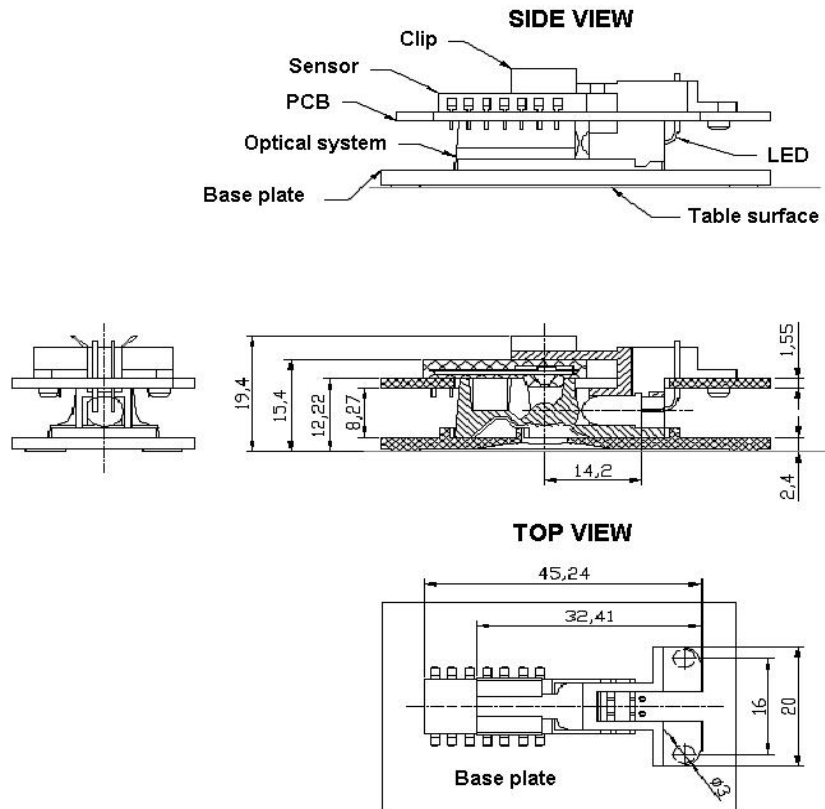
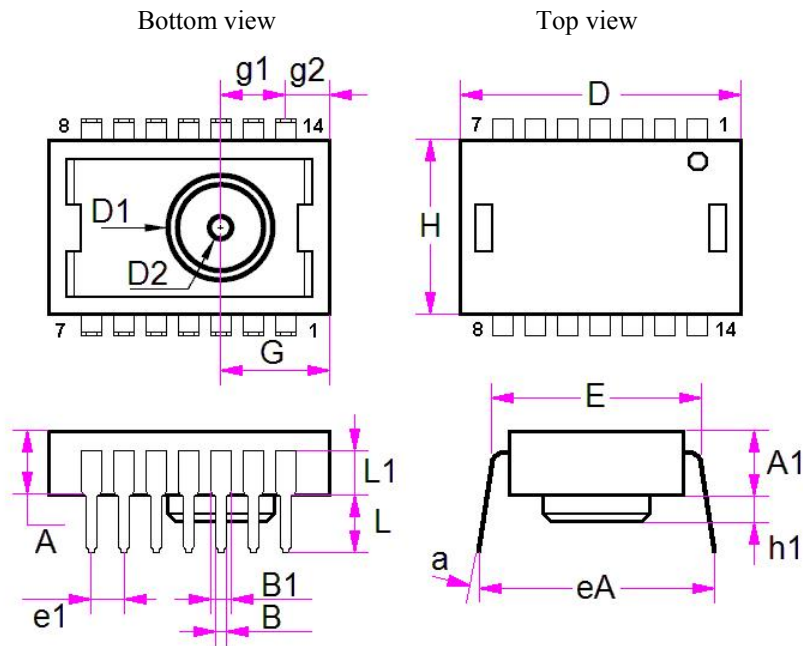
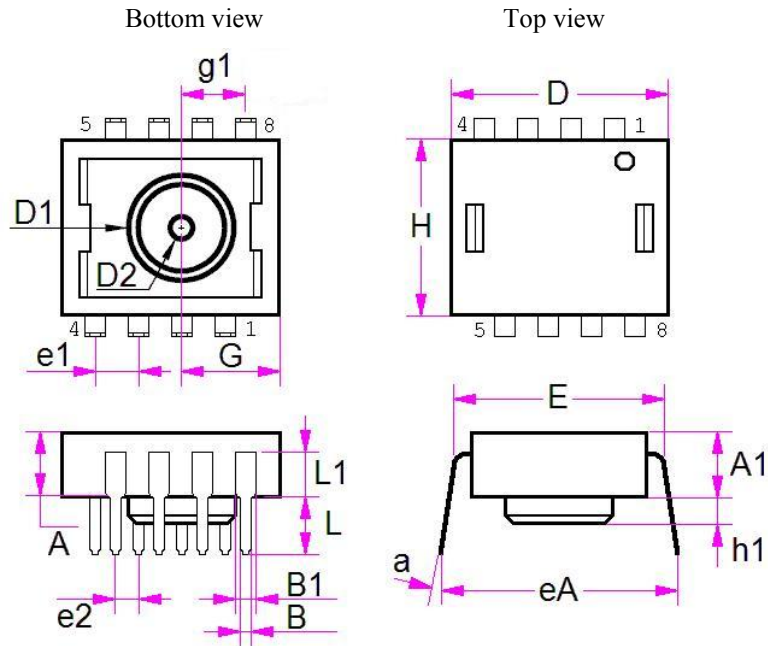


Fig. 17. Assembly drawing using Unique ICs optical system.



Symbol	D	H	A	A1	E	eA	e1	B	B1	L	L1	G	g1	g2	h1	D1	D2	a	
min	13.108	10.06	-	3.10	1376	14.02	-	-	0.916	3.18	2.08	5.234	3.543	1.17	1.32	5.5	0.4	0	
nom	13.208	10.16	3.20	3.20	13.96	14.22	1.778	0.457	1.016	3.28	2.18	5.334	4.064	1.27	1.42	5.6	0.8	-	
max	13.108	10.26	-	3.30	14.16	14.42	-	-	1.116	3.38	2.28	5.434	3.743	1.37	1.52	5.7	1.2	15	
unit	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	°

Fig. 18. Package outline drawing for UIC1003A.



Symbol	D	H	A	A1	E	eA	e1	e2	B	B1	L	L1	G	g1	h1	D1	D2	a	
min	9.80	9.0	-	3.08	10.35	12.25	-	-	-	0.80	2.87	2.08	4.35	2.90	1.32	5.5	0.4	0	
nom	9.90	9.1	3.18	3.18	10.60	12.35	2.00	1.00	0.457	0.90	2.97	2.18	4.45	3.00	1.42	5.6	0.8	-	
max	10.0	9.2	-	3.28	10.85	12.45	-	-	-	1.00	3.07	2.28	4.55	3.10	1.52	5.7	1.2	15	
unit	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	°

Fig. 19. Package outline drawing for UIC1003B.

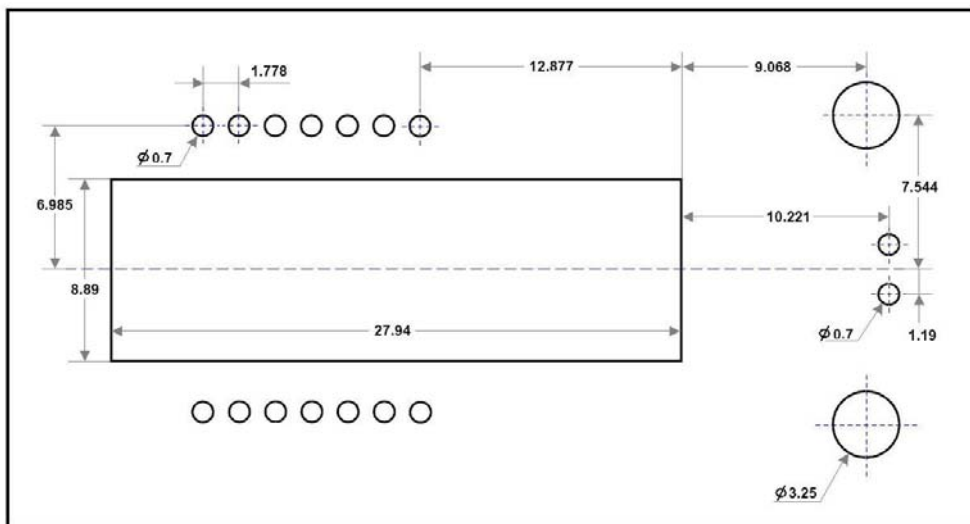
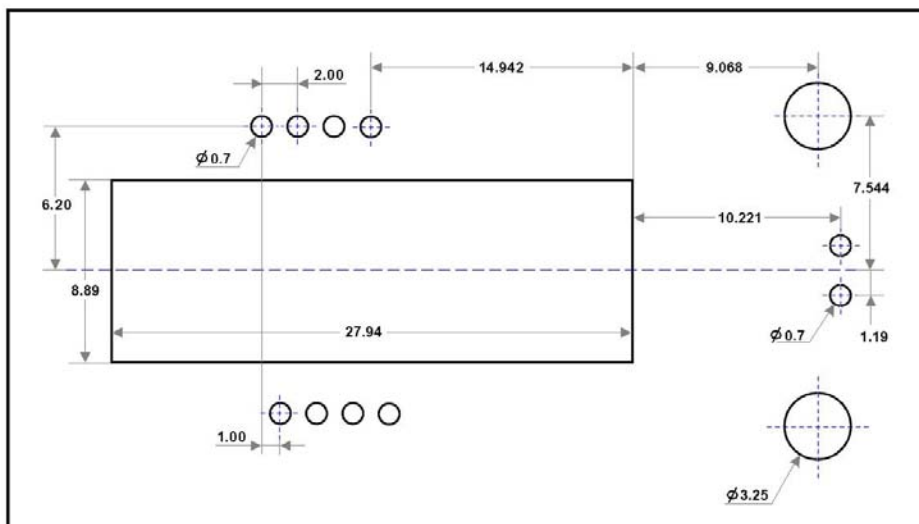


Fig. 20. Fragment of PCB recommended for mounting UIC1003A, optical system, LED and clip with Agilent optical system (top view).



**Fig. 21. Fragment of PCB recommended for mounting UIC1003B, optical system, LED and clip with Agilent optical system (top view).**

### **Design consideration concerning electrical circuit of UIC1003 using.**

Fig.22 shows a recommended typical UIC1003 application. The only block, which may require the elements nominal selection, is a clock generator using an elements C2, C3 and XT1. Nominal capacitance of C2, C3 depends on the type of a resonator used and on its frequency. If a quartz resonator is used capacitors C2, C3 in most cases are not need. If ceramic resonator is used nominal capacitance of C2, C3 amounts 10÷30 pF. Some types of ceramic resonators include required capacitors in its structure. Such resonators have additional middle output, which should be connected to a common circuit – GND. Elements C2, C3 and XT1 must be located on PCB as close as possible to appropriate pins of IC UIC1003A.

IC powering is performed from a single external voltage source  $VDD = +(2\div3.5) V$ . To decrease a crosstalk level filtering capacitor C6 with nominal capacitance 5÷20 uF must be connected to VDD circuit. Besides, IC UIC1003 has 3 internal supply circuits VDA, VDL and VD, which should be connected to filtering capacitors too. Filtering capacitor C4 should be ceramic one. As for C5, C6 the best result gives the use of tantalum capacitors owing to its low internal inductance, which ensures low total impedance at high frequencies. If aluminum capacitors are used they must be shunted by ceramic capacitors 0.1÷1 uF connected in parallel. Filtering capacitors C4÷C6 should be placed on PCB as close to corresponding power pins as possible. Circuits, connecting filtering capacitors with power pins, should be wide and short to ensure small parasitic inductance and resistance.

A common power bus – GND should have maximum possible width and square. In order to decrease noise and increase maximum achievable resolution it is desirable to use 2-layer PCB where one of the layers almost fully is used as GND-circuit.

Capacitor C1 specifies time constant of a power up reset circuit. Build in pull up resistor connected to pin R equals to 400 kΩ.

Light emitted diode D1 illuminates desktop surface and is powered from VDD. A negative lead of a LED is connected to the DAC output (pin QP), which determines the LED current value. IC UIC10003 enables usage of red and IR LED's. Among red LED's it may be recommended HLMP-ED80, which is most often used in optical mice because of high efficiency. But more high efficiency gives IR LED's. At other equal conditions IR LED may have current consumption 1.5÷2 times lower than red LED. From high efficiency IR LED's it may be recommended L-7113SF6C (working wavelength  $\lambda=860$  nm).

IC pins DAT and CLK are connected to external controller. Pin CLK is always an input one, pin DAT – is bidirectional. If controller is powered from another power source, than IC UIC1003, to agree input/output signal levels is need. In this case controller is programmed for operation with open collector type outputs and pins DAT and CLK are tied to VDD with resistors 1÷10 kΩ.

The last remark concerns output QP. It may be omitted. One of applications of output QP is an indication of normal working conditions when the brightness of the desktop is sufficient for normal optical mouse operation. If a red LED is connected between QP and GND through resistor 200÷1000 Ω it will light up at normal operation and become dim when the mouse is lifted up or the desktop is too dark. If LED is connected between VDD and QP (with the same resistor), it conversely will indicate when the mouse is lifted or operates on a too dark surface. For optical mouse with USB-interface any of two considered variants may be recommended. For wireless mouse any additional power consump-

tion is undesirable. For this reason only second variant can be recommended in this case.

IC UIC1003B application circuit differs from UIC1003A by absence of external generator circuits and RESET-circuit.

Some variants of IC UIC1003 applications together with external controller are given below.

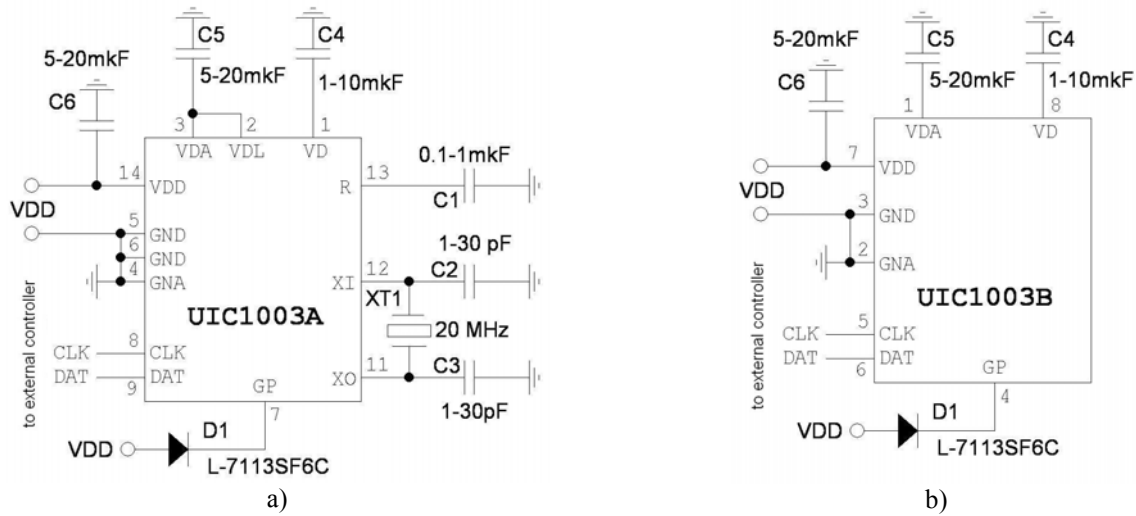


Fig. 22. Recommended typical application for UIC1003A (a) and UIC1003B (b).

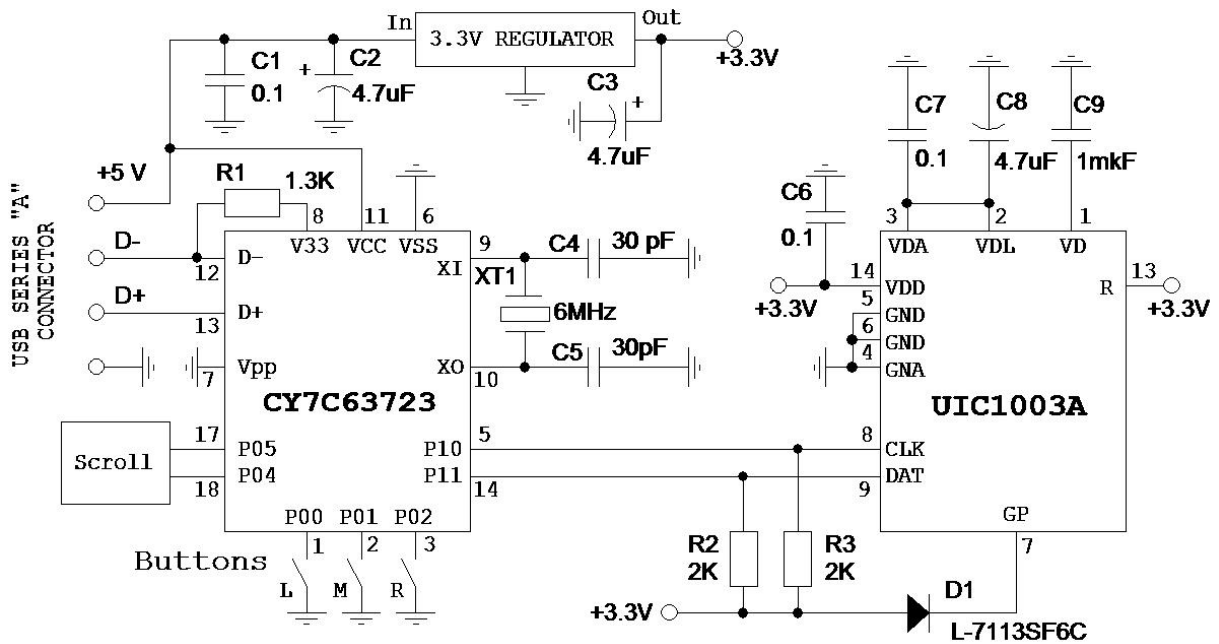


Fig. 23. Typical application in USB optical mouse using CY-PRESS controller and external +3.3 V voltage regulator.